AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claim 15 without prejudice.

1. (CURRENTLY AMENDED) A method of conditional branching in a pipelined processor, the method comprising the steps of:

(A) fetching a first instruction stored at a branch target address in response to encountering a branch instruction at a program counter address;

(B) decoding a second instruction stored at a next address adjacent said program counter address substantially simultaneously with said fetching; ~~and~~

(C) evaluating between (i) taking a branch defined by said branch instruction and (ii) not taking said branch substantially simultaneously with said fetching; and

(D) fetching a third instruction stored at a mispredict recovery address adjacent said next address in response to determining not to take said branch.

2. (CURRENTLY AMENDED) ~~The method of claim 1, further~~ A method of conditional branching in a pipelined processor, the method comprising the steps of:

(A) fetching a first instruction stored at a branch target address in response to encountering a branch instruction at a program counter address;

(B) decoding a second instruction stored at a next address adjacent said program counter address substantially simultaneously with said fetching;

(C) evaluating between (i) taking a branch defined by said branch instruction and (ii) not taking said branch substantially simultaneously with said fetching; and

(D) fetching a third instruction stored at a sequential instruction address adjacent said branch target address in response to determining to take said branch.

3. (PREVIOUSLY PRESENTED) The method of claim 2, further comprising the step of:

generating said sequential instruction address based upon said program counter address and a predetermined offset.

4. (CURRENTLY AMENDED) The method of claim ~~15~~ 1, further comprising the step of:

generating said misprediction recovery address based upon an exception program counter address and a predetermined offset.

5. (PREVIOUSLY PRESENTED) The method of claim 1, further comprising the step of:

generating said branch target address based upon said program counter address and an address displacement of said branch instruction.

6. (CURRENTLY AMENDED) The method of claim 1, further comprising the steps of:

generating a sequential instruction address adjacent said branch target address based upon said program counter address and a first predetermined offset;

generating a mispredict recovery address adjacent said next address based upon an exception program counter address and a second predetermined offset;

generating said branch target address based upon said program counter address and an address displacement of said branch instruction;

~~fetching a third instruction stored at said sequential instruction address in response to determining to take said branch;~~ and

fetching a fourth instruction stored at said mispredict recovery address in response to determining to not take said branch.

7. (PREVIOUSLY PRESENTED) A pipelined processor comprising:

a multiplexer; and

a circuit configured to present (i) a branch target address based on a branch instruction stored at a program counter address in prediction of taking a branch, (ii) a sequential instruction address having a first value adjacent said program counter address and (iii) a mispredict recovery address to said multiplexer substantially simultaneously.

8. (PREVIOUSLY PRESENTED) The pipelined processor of claim 7, wherein said circuit is further configured to present said sequential instruction address having a second value adjacent said branch target address to said multiplexer in response to determining to take said branch.

9. (CURRENTLY AMENDED) The pipelined processor of claim 7, wherein said circuit comprises:

a prefetch program counter for storing an address presented by said multiplexer among said branch target address, said sequential instruction address and said ~~misdirect~~ mispredict recovery address.

10. (PREVIOUSLY PRESENTED) The pipelined processor of claim 7, wherein said circuit comprises:

an instruction register for storing said branch instruction.

11. (PREVIOUSLY PRESENTED) The pipelined processor of claim 7, wherein said circuit comprises:

an exception program counter disposed in a decode stage of said pipelined processor for storing an exception program counter address used upon determining not to take said branch.

12. (PREVIOUSLY PRESENTED) The pipelined processor of claim 7, wherein said circuit comprises:

an exception program counter disposed in an execution stage of said pipelined processor for storing an exception program counter address used upon determining not to take said branch.

13. (PREVIOUSLY PRESENTED) The pipelined processor of claim 7, wherein said circuit comprises:

a prefetch program counter for storing said program counter address;

an instruction register for storing said branch instruction; and

an exception program counter for storing an exception program counter address used in generating said mispredict recovery address having a second value proximate said program counter address.

14. (CURRENTLY AMENDED) A pipelined processor comprising~~,~~:

means for decoding a first instruction stored at a next address adjacent a program counter address;

means for fetching a second instruction stored at a branch target address substantially simultaneously with said decoding in response to encountering a branch instruction at said program counter address; ~~and~~

means for evaluating between (i) taking a branch defined by said branch instruction and (ii) not taking said branch substantially simultaneously with said fetching; and

means for fetching a third instruction stored at a mispredict recovery address adjacent said next address in response to determining not to take said branch.

15. (CANCELED)

16. (PREVIOUSLY PRESENTED) The method of claim 1, further comprising the step of:

storing said program counter address in a stage of said pipelined processor for at least two cycles.

17. (PREVIOUSLY PRESENTED) The pipelined processor of claim 13, wherein said circuit further comprises:

an incrementor coupled to said prefetch program counter and configured to generate said sequential instruction address from said program counter address.

18. (PREVIOUSLY PRESENTED) The pipelined processor of claim 13, wherein said circuit further comprises:

an adder (i) coupled to both said prefetch program counter and said instruction register and (ii) configured to generate said branch target address by adding said program counter address to an address displacement of said branch instruction.

19. (PREVIOUSLY PRESENTED) The pipelined processor of claim 13, wherein said circuit further comprises:

an incrementor coupled to said exception program counter and configured to generate said mispredict recovery address.

20. (PREVIOUSLY PRESENTED) The pipelined processor of claim 13, wherein said exception program counter is coupled to said prefetch program counter to receive said program counter address.